A Novel Design of a McCulloch-Pitts Neuron in CMOS VLSI

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Abstract

Due to the advancement in recent hardware technology and vast information availability, a growing need for efficient and adaptable processing has become a necessity. Artificial neural network (ANN) mimics the functionality of human brain and can be applied to solve many complex engineering problems such as pattern recognition, control, time series modeling, and optimization. The capability of ANN is limited due to current microprocessing systems, and thus need specialized digital logic. In this paper, a neuron for a multilayer preceptron (MLP) using back-propagation is applied using digital logic methods, which is implemented using CMOS very large system integration (VLSI) for high speed and energy efficiency is proposed. The key feature, massive parallel processing is made possible using the proposed ANN approach and as proof-of-concept.

Introduction

Artificial Neural Networks (ANNs) mimic the function of a biological neural network. When considering the biological neural network at a very summarized view point, their function is pattern recognition. Humans use their brains to recognize patterns in all sorts of things, from mathematics, to weather, survival, etc. Now as expected, ANNs attempt to mimic this activity, and can therefore be used for similar tasks, such as pattern recognition, prediction, controls, outlier detection, etc. These basic categories encompass many engineering situations that would otherwise require complex mathematics, very specialized programming, or the “human touch”.

If implemented properly the Programmable Artificial Neural Chip Acquires Knowledge by Experience (PANCAKE) could have many potential uses. It’s main advantage is that it can be implemented as a control system that operates on a large amount of variables. One potential application is increasing the accuracy of readings from nerve endings for motor enhanced prosthetics. The propagation of nerve signals can be effected by both internal and external factors[1]. Do to this variance, the quality of motor controllers will vary. Implementing PANCAKE with appropriate sensors (IE Body temp, Heart rate, Barometric Pressure) will allow for the signal to be automatically compensated, and therefore will increase the quality of control.

Another potential application for PANCAKE would be implementation in prediction systems. For example PANCAKE could monitor a large variety of environmental weather conditions, and from that data, it could begin to make localized weather prediction on rain fall, humidity, et cetera. PANCAKE can also use it's large amount of inputs for tasks such as pattern recognition which might be geared for industrial quality detection, character detection, and so on.

The key component of ANNs are the neurons themselves. A typically accepted neuron structure is the McCulloch-Pitts neuron(MPN)[1]. The MPN consists of weights, a summation, and an activation function as seen in Figure 1. The MPN applies weights to incoming signals, and sums the weighted signals. That summation is fed into an activation function ϕ, which is commonly assigned the sigmoid logistics function in Equation 1 where v_j is defined as the output of the summing function.

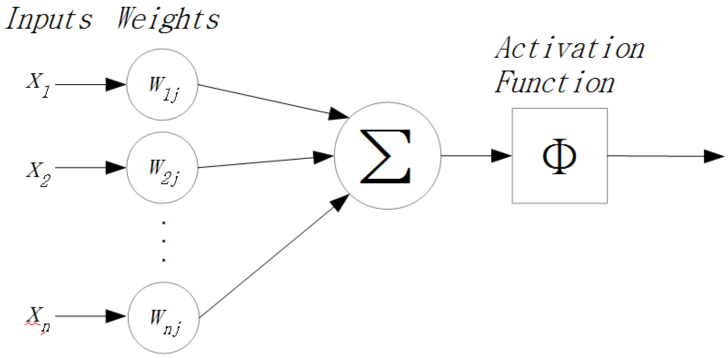


Figure 1: A McCulloch-Pitts neuron

$$\phi_j = \frac{1}{1 + e^{-v_j}} \tag{1}$$

Using a learning algorithm such as back-propagation, a network of MPNs can be taught to handle sets of data, and make predictions or choices based on past experience. The individual neurons "learn" by adjusting their attached weights according to feedback from the learning algorithm.

The proposed neuron is a single piece in an integrated circuit containing a discrete artificial neural network capable of multiple different machine learning tasks. Since PANCAKE implements a neural network in hardware form, it will be capable of multiple different machine learning tasks, and capable of handling assigned tasks in a true parallel nature.

Methodology

MLP consist of three parts as shown in Figure 2, Weights, Summing Compression Adder (SCA), and the Sigmoid Function Block (SFB). The topology of these functional blocks will be described in this section.

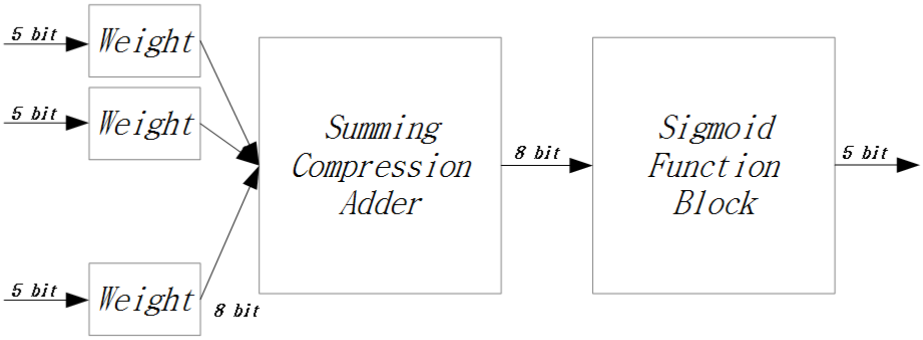
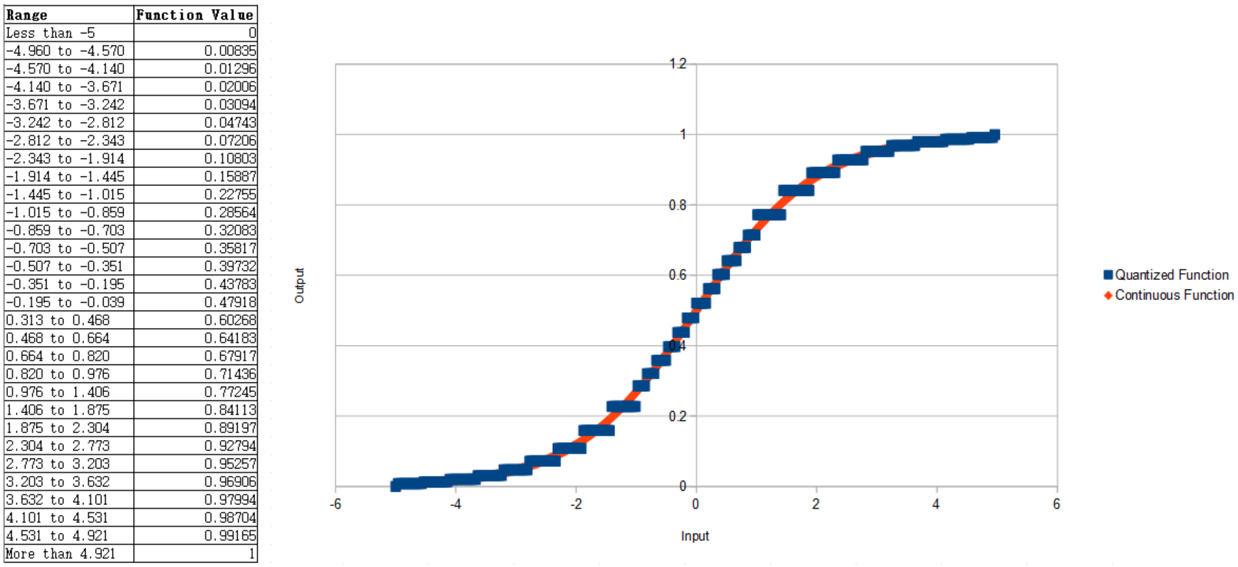


Figure 2: A McCulloch-Pitts neuron

The system is discrete, and requires the SFB to quantize the continuous data into 32 states as shown in Figure 3.



Range	Function Value
Less than -5	0
-4.960 to -4.570	0.00835
-4.570 to -4.140	0.01296
-4.140 to -3.671	0.02006
-3.671 to -3.242	0.03094
-3.242 to -2.812	0.04743
-2.812 to -2.343	0.07206
-2.343 to -1.914	0.10803
-1.914 to -1.445	0.15887
-1.445 to -1.015	0.22755
-1.015 to -0.859	0.28564
-0.859 to -0.703	0.32083
-0.703 to -0.507	0.35817
-0.507 to -0.351	0.39732
-0.351 to -0.195	0.43783
-0.195 to -0.039	0.47918
0.313 to 0.468	0.60268
0.468 to 0.664	0.64183
0.664 to 0.820	0.67917
0.820 to 0.976	0.71436
0.976 to 1.406	0.77245
1.406 to 1.875	0.84113
1.875 to 2.304	0.89197
2.304 to 2.773	0.92794
2.773 to 3.203	0.95257
3.203 to 3.632	0.96906
3.632 to 4.101	0.97994
4.101 to 4.531	0.98704
4.531 to 4.921	0.99165
More than 4.921	1

Figure 3: A table and graph displaying the discrete and continuous sigmoid function

Binary values are assigned to defined points on the input axis, as well as the output axis. The input is cut into the signed binary value 00000000 to 11111111, or more simply an 8 bit input. The output is defined as a 5 bit output. From these assigned values, Karnaugh maps can be made to find the boolean relation[4]. These functions are later translated into a NAND-NOR system and then further translated into a VLSI Block. Functions 2 to 6 are defined assuming the most significant bit of the input is A and the least significant bit is H.

$$MSB = \bar{A} \tag{2}$$

$$MSB^{-1} = \bar{A}B + BD + BC + \bar{A}CDH + \bar{A}CDG + \bar{A}CDF + \bar{A}CDE \tag{3}$$

$$\begin{aligned} MSB^{-2} = {} & \bar{A}C\bar{D} + \bar{A}BC + ACD + \bar{B}C\bar{D}F + \bar{B}C\bar{D}E + AB\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}DG + \bar{A}\bar{B}\bar{C}DF \\ & + \bar{A}\bar{B}\bar{C}DE + \bar{B}C\bar{D}GH + \bar{A}\bar{C}DEFG + \bar{A}C\bar{E}\bar{F}\bar{G}\bar{H} + C\bar{D}EFGH \end{aligned} \tag{4}$$

$$\begin{aligned} MSB^{-3} = {} & \bar{C}\bar{D}EF + \bar{A}\bar{B}C\bar{D} + BCDE + A\bar{B}\bar{C}D + AB\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}DEH + \bar{A}\bar{B}\bar{C}EG \\ & + \bar{A}\bar{C}EF\bar{G} + \bar{A}B\bar{C}E\bar{F} + \bar{A}B\bar{C}D\bar{E} + A\bar{B}DEH + A\bar{B}DEG + A\bar{B}DEF \\ & + AB\bar{D}E\bar{F} + AB\bar{D}E\bar{G} + AB\bar{D}E\bar{H} + \bar{A}\bar{C}D\bar{E}\bar{F}\bar{G} + \bar{B}C\bar{D}\bar{E}\bar{F}\bar{G} + \bar{B}C\bar{D}\bar{E}\bar{F}\bar{H} \\ & + \bar{A}BD\bar{E}FH + \bar{A}BD\bar{E}FG + \bar{A}\bar{B}D\bar{E}\bar{F}\bar{G}\bar{H} + AB\bar{D}\bar{E}FGH \end{aligned} \tag{5}$$

$$\begin{aligned} MSB^{-4} = {} & \bar{A}\bar{B}\bar{D}FH + \bar{C}\bar{D}\bar{E}FH + \bar{A}\bar{B}\bar{D}FG + \bar{A}\bar{C}\bar{E}FG + \bar{A}\bar{B}C\bar{D}E + \bar{A}C\bar{D}EG \\ & + \bar{A}\bar{B}CEF + \bar{A}C\bar{D}EF + \bar{A}B\bar{C}\bar{D}\bar{E} + A\bar{B}\bar{C}E\bar{F} + A\bar{B}\bar{C}DE + A\bar{B}CD\bar{E} + ACD\bar{E}F \\ & + AB\bar{C}\bar{D}E + ABDEF + ABCF\bar{G} + ABCF\bar{H} + \bar{B}\bar{C}\bar{E}FGH + \bar{B}\bar{C}E\bar{F}\bar{G}\bar{H} \\ & + \bar{A}\bar{B}\bar{C}D\bar{F}\bar{G} + \bar{B}C\bar{D}EFG + \bar{A}CEFGH + \bar{A}B\bar{C}\bar{E}GH + \bar{A}B\bar{C}DF\bar{G} \\ & + \bar{A}B\bar{C}DE\bar{F} + \bar{A}BCD\bar{E}\bar{F} + A\bar{B}\bar{C}\bar{D}\bar{E}H + A\bar{B}\bar{C}\bar{D}\bar{E}G + A\bar{B}\bar{C}\bar{D}\bar{E}F \\ & + A\bar{B}C\bar{E}\bar{F}\bar{G} + A\bar{B}C\bar{E}\bar{F}\bar{H} + ABC\bar{D}\bar{E}\bar{F} + \bar{A}\bar{B}D\bar{E}\bar{F}\bar{G}\bar{H} + \bar{A}BD\bar{E}F\bar{G}\bar{H} \\ & + BC\bar{D}E\bar{F}GH + A\bar{B}DE\bar{F}\bar{G}\bar{H} \end{aligned} \tag{6}$$

Next, the SCA is considered. One of the issues presented in PANCAKE is that the network is defined to be 32 x 32 neurons; implying that each neuron will have 32 connections. This also implies that the summation node of the neuron will have to sum 32 8 bit numbers in a parallel fashion. Though this is entirely achievable the output of the adder would be a 13 bit number, and would require more inputs to be considered in the SFB. Also the adder circuit as well as the SFB will be larger and will hinder the goal of 32x32 neurons. Therefore the following design is proposed in Figure 4. The concept is to use an 8 bit full adder to add two 8 bit numbers, and *ignore* the LSB. Instead the carry bit is treated as the MSB of the output byte, in essence shifting each bit down one binary value. This method can be cascaded to handle any amount of inputs and compress it into an 8 bit output.

It should be noted that if an SCA is not utilized to full capacity, there will be a more significant round off error (IE an SCA is build to handle 10 inputs, but only 5 are used). If this case is not avoidable, then selector logic must be used to take intermediate sums from the SCA to reduce error.

Lastly, the Weight block will be discussed. A typical weight in an ANN operates as a gain, or “multiplier” to it’s input data. Conventional multiplication will not work well within the bounds

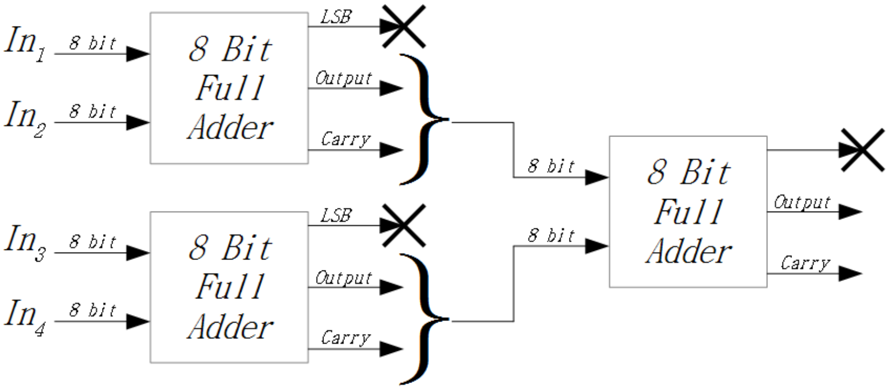


Figure 4: A block diagram of a four 8 bit input, single 8 bit output Summing Compression Adder

of the discrete domain defined for the designed neuron. The weight block is instead designed to operate on a shift-and-add system. The back-propagation learning algorithm will have to be modified to generate two values, one that specifies how many bits the value will have to shift and in what direction. The second value will be a "fine tune" adjustment to specify a value to add or subtract from the shifted input.

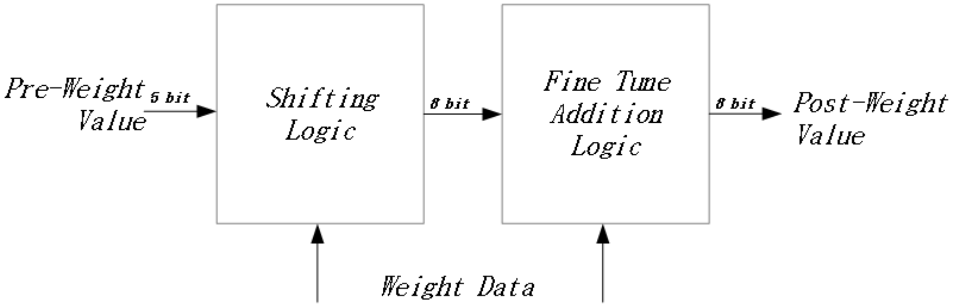


Figure 5: A block diagram of the weight node

Results and Analysis

All of the systems proposed are within the realm of possibility to implement, however their success depends on the implementation of optimal learning algorithm. The SFB is designed in Electric VLSI using the sea of gates layout method[3]. The speed of the largest gate in the SFB is measured in a SPICE simulation, and is found to be a 19.2 nS Transition, or alternatively, it is capable of switching at 51 MHz when used alone. The dimensions of the SFB are measured to be 1320 nM by 1120 nM.

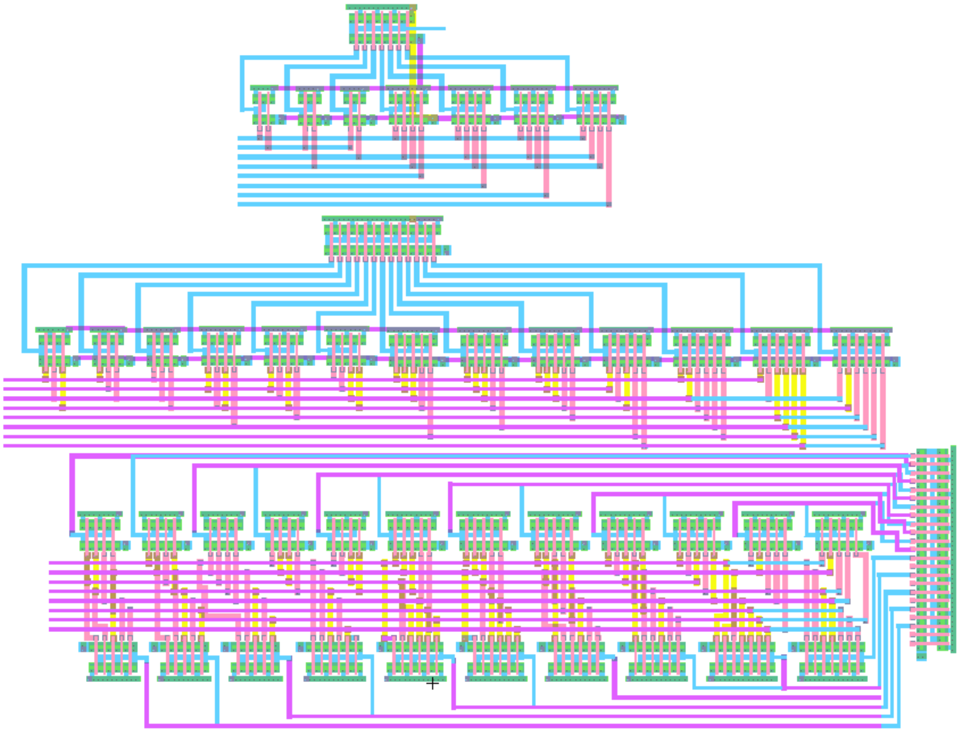


Figure 6: A section of the completed SFB

Conclusion and Future Work

PANCAKE is modeled based on the state-of-the art methods tailored to solve real-world constraints. The proposed architecture is feasible, and require testing on benchmark problems such as weather prediction, which will be discussed in future research.

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